## REMARKS

The Examiner's Action mailed on August 16, 2006, has been received and its contents carefully considered. Additionally attached to this Amendment is a Petition for a One-month Extension of Time, extending the period for response to December 16, 2006.

In this Amendment, Applicants have amended claims 35-37 and added new claims 38-41. Claim 35 is the sole independent claim, and claims 35-41 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 35-37 were rejected for non-statutory obviousness-type double patenting over an earlier patent to *Kodama et al.* (US 6,642,916 B1, henceforth the *'916* patent). This rejection is respectfully traversed.

The Office Action alleges that "all the claimed limitations are encompassed by the claimed limitations in US 6,642,916". However, the *'916* patent does not claim "said signals representing picture-element intensities alternate between potentials on one side of a certain center potential and potentials on an opposite side of said center potential at predetermined intervals, *a plurality of said first signal lines being driven consecutively to the active level during each of said predetermined intervals*" (emphasis added), as presently recited in claim 35, for example, and all the remaining claims depend directly or indirectly from claim 35. Claims 35-37 are therefore not obvious over the *'916* patent.

Notwithstanding the above, a Terminal Disclaimer is filed herewith, which overcomes the rejection.

Claims 35 and 37 were rejected under 35 USC §103(a) as obvious over Applicants' Prior Art FIG. 1-3 and supporting parts of the present specification in combination with *Hayashi et al.* (US 5,818,413), and claim 36 was rejected under 35 USC §103(a) as obvious over this combination further in view of *Kitamura* (US 5,682,175). These rejections are respectfully traversed.

Claim 35 has been amended for clarity, and presently recites "said signals representing picture-element intensities alternate between potentials on one side of a certain center potential and potentials on an opposite side of said center potential at predetermined intervals, *a plurality of said first signal lines being driven consecutively to the active level during each of said predetermined intervals*" (emphasis added).

Claims 36 and 37 have been amended to cover both the short-circuiting method illustrated in FIG. 5 and FIG. 14 and the method illustrated in FIG. 4 and FIG. 11 of connecting the signal lines in question to a fixed potential. New claims 38-41 describe these specific methods.

The present application is based on the seventh embodiment, described in a non-limiting example from page 14, line 19, to page 15, line 15, and illustrated in FIG. 10.

Briefly, a second signal line or source line is driven in one direction while a plurality of first signal lines or gate lines are active, then driven in the opposite

direction while a next plurality of first signal lines are active, and so on. In the example of FIG. 10, the driving direction changes at intervals of three gate lines (three horizontal raster lines on the liquid crystal display screen).

In Applicants' admitted Prior Art, (page 1, lines 24-26, Fig, 3, and page 6, line 31. to page 7, line 27), a second signal line is driven in one direction while one first signal line is active, then driven in the opposite direction while the next first signal line is active, and so on, the driving direction changing at intervals of only one gate line or raster line.

As noted on page 15, lines 1-6, switching driving directions only once every three gate lines (or more generally, once every N gate lines, where N is any integer greater than one) reduces current consumption.

This source line driving scheme that reverses polarity at intervals of N instead of intervals of one is not taught or suggested in the cited references. *Hayashi et al.* is entirely concerned with schemes for driving the gate lines (X in Fig. 1A) and says nothing about how the source lines (Y in Fig. 1A) are to be driven. *Kitamura* discusses source line driving but says nothing about alternating the polarity of the driving signals.

*Hayashi et al.* shows a scheme in which two adjacent gate lines are driven to the active level simultaneously, but they are not driven consecutively to the active level, only one being active at a time, as required by amended claim 35.

The Office Action refers on page 5 thereof to FIG. 1B (a schematic of the vertical-scanning circuit **1**) and column 5, lines 26-31 of *Hayashi et al.*, which reads as follows:

> The vertical-scanning circuit **1** has switching means for controlling the switching of the sequential output of selection pulses to adjust the number of lines to be selected in a horizontal-scanning period according to the specification of video signals.

However, although the selection pulses may be outputted sequentially, the number of lines selected to be scanned are scanned simultaneously and *not* sequentially. This is made clear in the Summary of the Invention, see column 2, line 45 - column 3, line 11:

> To solve the above-described technical problems in the conventional apparatuses, it is an object of the present invention to provide, in a display apparatus with a full-frame structure designed for displaying computer outputs such as a VGA signal, a circuit enabling a TV signal to be also displayed. In other words, it is an object of the present invention to provide a display apparatus which allows both interlaced drive shown in FIG. 16 and noninterlaced drive shown in FIG. 19 or FIG. 20 simply by internal switching operations. To achieve the foregoing object, the following measures are taken. A display apparatus according to the present invention basically comprises arrayed pixels, a vertical-scanning circuit, and a horizontal-scanning circuit. The vertical-scanning circuit sequentially outputs selection pulses and line-sequentially scans pixels in one vertical-scanning period. The horizontal-scanning circuit transmits and writes a video signal in one horizontal-scanning period into the pixel lines selected with the sequential scanning. It is a feature of the apparatus that the vertical-scanning circuit includes switching means for controlling the switching of the selection pulses sequentially output and adjusts the number of pixel lines to be selected in a horizontal-scanning period according to the standard of the video signal. The following describes operations precisely. The switching means enables a noninterlaced drive to be performed for one frame in one vertical-scanning period by selecting one line in every horizontal-scanning period when a video signal conforming to the noninterlace standard is input. *The switching means enables an interlaced drive to be performed for one field in one vertical-scanning period by selecting two lines at the same time in every horizontal-scanning period when a video signal conforming*

*to the interlace standard is input, and shifts the simultaneously selected two lines by one line in every field.* (*emphasis added*)

Consequently, neither Applicants' admitted Prior Art, nor *Hayashi et al.,* nor *Kitamura* , whether taken separately or in combination, teaches or suggests "said signals representing picture-element intensities alternate between potentials on one side of a certain center potential and potentials on an opposite side of said center potential at predetermined intervals, *a plurality of said first signal lines being driven consecutively to the active level during each of said predetermined intervals*" (emphasis added) as recited in independent claim 35.

Accordingly, amended claim 35 patentably defines over the Applicant's admitted Prior Art and the cited references, whether taken separately or in combination, and is therefore allowable.

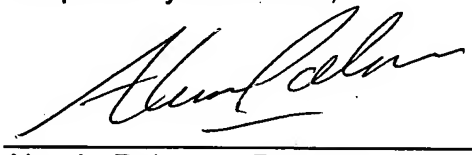
Amended claims 36 and 37 and newly added claims 38-41 are also allowable at least due to their dependence on claim 35.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should the remittance be accidentally missing or insufficient, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,



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Date

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